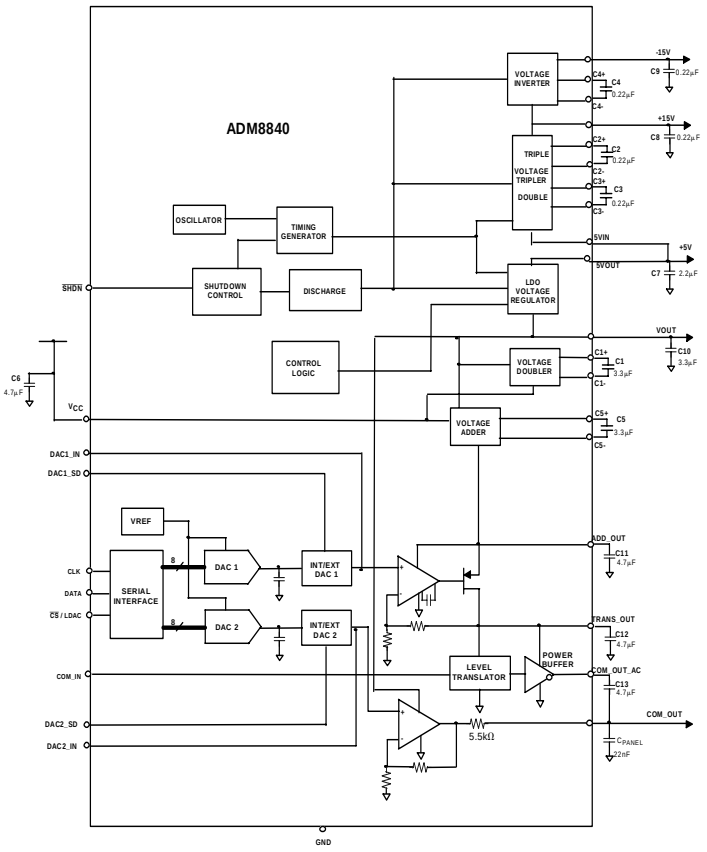
# Charge Pump Regulator & COM Driver for Color TFT Panel

## Preliminary Technical Data — ADM8840

**FEATURES**
**Programmable COM Driver to prevent Screen-Burn**
**3 Voltages (5.0V,15.0V,-15.0V) from one 3V Supply**
**Power Efficiency optimised for use with TFT in mobile phones**
**Low Quiescent Current**
**Low Shutdown Current (<5uA)**
**Shutdown Function**

**APPLICATIONS**
**Handheld Instruments**
**TFT LCD Panels**
**Cellular Phones**

**FUNCTIONAL BLOCK DIAGRAM**




### GENERAL DESCRIPTION

The ADM8840 combines a charge pump regulator and a Common Line (COM) driver in a single chip solution for use in TFT LCD's. The device provides an LCD controller and grayscale DAC supply voltage of 5.0V (±2%), 2 gate drive voltages of +15V and -15V and a COM driver voltage. This COM Driver voltage alternates the polarity of the Common line voltage every line (or every frame) on the display in order to prevent screen-burn occuring over time. The ADM8840 is powered by a single 3.0V supply.

The ADM8840 has an internal 100KHz oscillator for driving the charge pumps.

The COM Driver section of the ADM8840 can be used to generate the alternate frame or line inversion of the COM line of the LCD panel. The ADM8840 receives the COM clock from the controller with a frequency up to 10kHz and allows programmable conditioning of its amplitude and centre voltage through the use of on-board DAC's. This allows programmable elimination of display flicker caused by the COM inversion.

The COM_OUT amplitude can be programmed from 4.0V to 7.0V in steps of 28mV. The COM_OUT centre voltage can be programmed to 0.9V to 2.8V in steps of 14mV.

The ADM8840 provides power up sequencing of the -15V and +15V gate drive outputs, ensuring the -15V starts to power up before the +15V.

The ADM8840 has a number of power save features, including low power Shutdown. The 5.0V output consumes the most power, so Power Efficiency is also maximised on this output with an oscillator enabling scheme (Green Idle™).

The ADM8840 is fabricated using CMOS technology for minimal power consumption. The part is packaged in a 32-pin LFCSP package.

™ Green Idle is a registered trademark of Analog Devices Inc.

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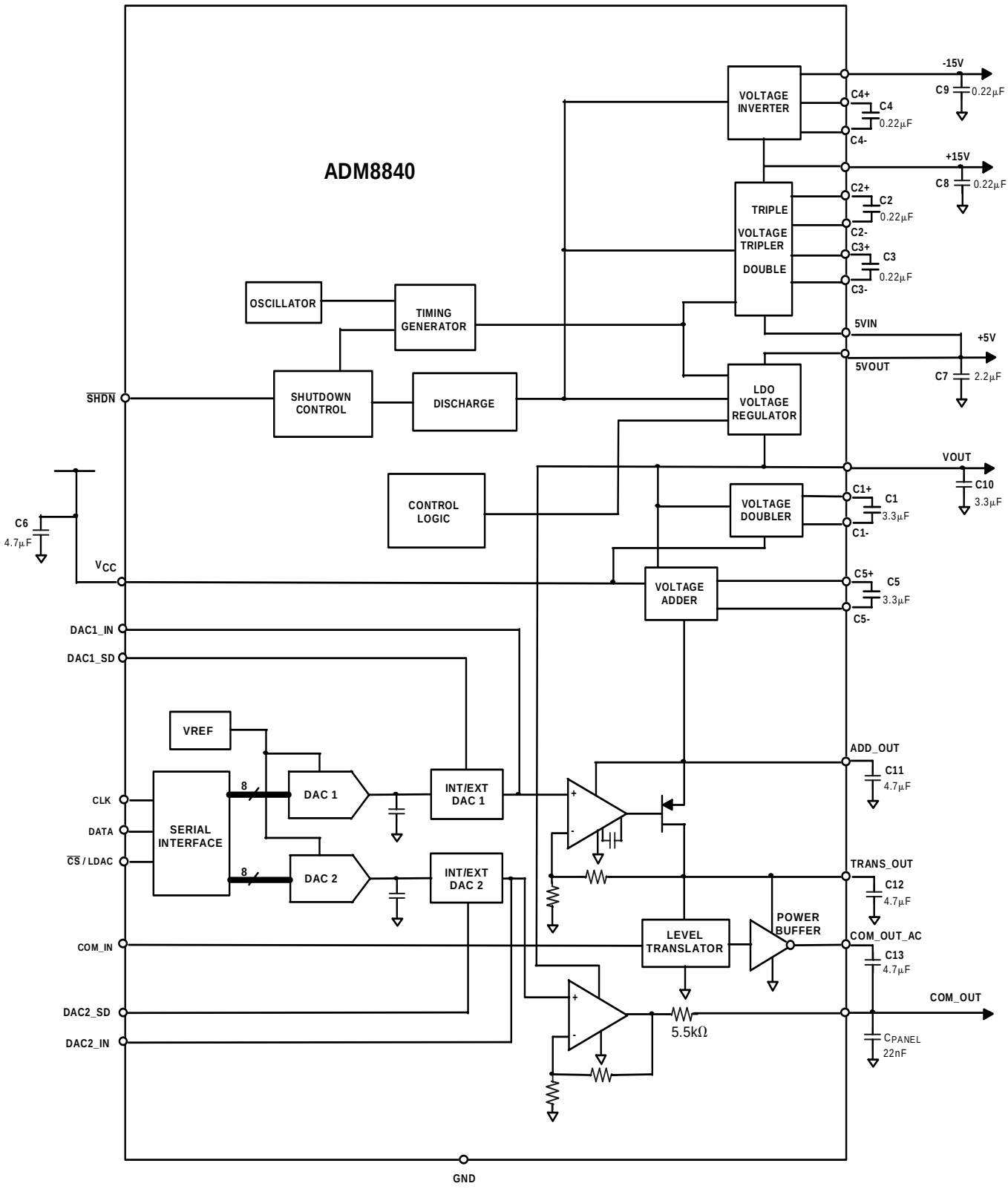
# ADM8840




**ADM8840 FUNCTIONAL BLOCK DIAGRAM**

($V_{CC}$ = +3V-10%,+20%, $T_A$=-40°C to +85°C unless otherwise noted )
C1,C5,C10=3.3µF; C2,C3,C4,C8,C9=0.22µF; C6,C11,C12,C13=4.7µF; C7 =2.2µF

# ADM8840-SPECIFICATIONS

| PARAMETER | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| Input Voltage,$V_{CC}$ | 2.7 | 3.3 | 3.6 | V | |
| Supply Current,$I_{CC}$ | | 750 | | uA | O/Ps Unloaded; COM_IN Low; DAC1_SD, DAC2_SD Low |
| | | 5 | | uA | Shutdown Mode DAC1_IN and DAC2_IN should be open circuit because there is a voltage on these pins due to the output of the DAC. |
| **CHARGE PUMP REGULATOR** | | | | | |
| **+5.0V OUTPUT** | | | | | |
| Output Voltage | 4.9 | 5.0 | 5.1 | V | $I_L$ = 10uA to 5mA |
| Output Current | | | 5 | mA | |
| Output Ripple | | 10 | | mV p-p | 5mA load |
| Transient Response | | 5 | | us | $I_L$ stepped from 10uA to 5mA |
| **+15.0V OUTPUT** | | | | | |
| Output Voltage | 14.0 | 15.0 | 16.0 | V | $I_L$ = 1uA to 100uA |
| Output Current | | 50 | 150 | uA | |
| Output Ripple | | 50 | | mV p-p | $I_L$=100uA |
| **-15.0V OUTPUT** | | | | | |
| Output Voltage | -16.0 | -15.0 | -14.0 | V | $I_L$ = -1uA to -100uA |
| Output Current | -150 | -50 | | uA | |
| Output Ripple | | 50 | | mV p-p | $I_L$=-100uA |
| Charge-Pump Frequency | TBD | 100 | TBD | kHz | |
| **DIGITAL INPUT PINS** | | | | | |
| Input Voltage, $V_{IH}$ | 0.7$V_{CC}$ | | | V | |
| | | | 0.3$V_{CC}$ | V | |
| Digital Input Current | | | 1 | µA | |
| Digital Input Capacitance | | | 10 | pF | Note 1. |
| **COM DRIVER** | | | | | |
| COM_OUT | | | | | |
| Amplitude | 4 | | 7 | V | |
| Amplitude Stepsize | | 28 | | mV | |
| Amplitude Accuracy | | <10% | | % | $V_{COM\_OUT}$=5V; DAC1 loaded with preset values; Measured at TRANS_OUT DAC1 preset values is 1V and Vcom should be 6V |
| Center Voltage | 0.9 | 1.8 | 2.8 | V | |
| Center Voltage Stepsize | | 14 | | mV | |
| Center Voltage Accuracy | | <10% | | % | $V_{CENTER}$=1.8V; DAC2 loaded with preset values DAC2 preset values is 500mV and Vcentre should be 1.5V. |
| Rise/Fall Time | | 1 | | µs | $C_{PANEL}$=20nF |
| Center Voltage Settling Time | | TBD | | us | |
| **PANEL** | | | | | |
| Load Capacitance | | 20 | | nF | |
| **POWER EFFICIENCY** | | 70 | | % | $5V_{OUT}$ Load = 5mA; +/-15V Load = +/-100uA; COM_IN Freq = 10kHz; $C_{PANEL}$ = 20nF; Vcc=2.7V; Note 2 |

NOTES
1. Guaranteed by Design. Not 100% Production Tested.
2. COM Driver load is defined as the load current flowing through C13 with DACs loaded with preset values.
* Specifications are target values and are subject to change without notice.

# ADM8840

## Timing Specifications

$V_{CC}$ = +3V-10%,+20%, $T_A$=-40°C to +85°C

| PARAMETER | Min | Typ | Max | Units | Test Conditions /Comments |
|---|---|---|---|---|---|
| POWER-UP SEQUENCE | | | | | |
| 5V Rise time, $T_{R5V}$ | | TBD | | us | 10% to 90%, Figure 2 |
| +15V Rise time, $T_{R15V}$ | | TBD | | ms | 10% to 90%, Figure 2 |
| -15V Fall time, $T_{F15V}$ | | TBD | | ms | 90% to 10%, Figure 2 |
| Delay between $V_{CC}$ rise and SHDN rise, $T_{DELAY1}$ | | TBD | | ms | Figure 2 |
| Delay between -15V fall and +15V rise, $T_{DELAY2}$ | | TBD | | ms | Figure 2 |
| POWER- DOWN SEQUENCE | | | | | |
| 5V Fall time, $T_{F5V}$ | | TBD | | ms | 90% to 10%, Figure 2 |
| +15V Fall time, $T_{F15V}$ | | TBD | | ms | 90% to 10%, Figure 2 |
| -15V Rise time, $T_{R15V}$ | | TBD | | ms | 10% to 90%, Figure 2 |
| SERIAL INTERFACE | | | | | |
| t1 | | TBD | | ns | CS/LDAC falling edge to SCLK Rising Edge; Note 1; Note2 |
| t2 | | TBD | | ns | SCLK High Pulsewidth; Note 1; Note2 |
| t3 | | TBD | | ns | SCLK Low Pulsewidth; Note 1; Note2 |
| t4 | | TBD | | ns | Minumum CS/LDAC high time; Note 1; Note2 |
| t5 | | TBD | | ns | SCLK Rising Edge to CS/LDAC Rising Edge; Note 1; Note2 |
| t6 | | TBD | | ns | DATA Setup time; Note 1; Note2 |
| t7 | | TBD | | ns | DATA Hold time; Note 1; Note2 |

NOTES
1. Guaranteed by Design. Not 100% Production Tested.
2. See Timing Diagram in Figure 4.
* Specifications are target values and are subject to change without notice.

### ABSOLUTE MAXIMUM RATINGS*

(TA=25°C unless otherwise noted.)

| | |
|---|---|
| Supply Voltage | -0.3 V to +4.0 V |
| Input Voltage on Digital Inputs | -0.3 V to +4.0 V |
| Output Short Circuit Duration to GND | 10 seconds |
| Output Voltage | |
| +5.0V Output | -0.3 V to +6.0 V |
| -15.0V Output | -17 V to +0.3 V |
| +15.0V Output | -0.3 V to +17 V |
| Operating Temperature Range | -40°C to +85°C |
| Power Dissipation | 50mW |
| Storage Temperature Range | -65°C to +150°C |
| ESD | Class I |

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

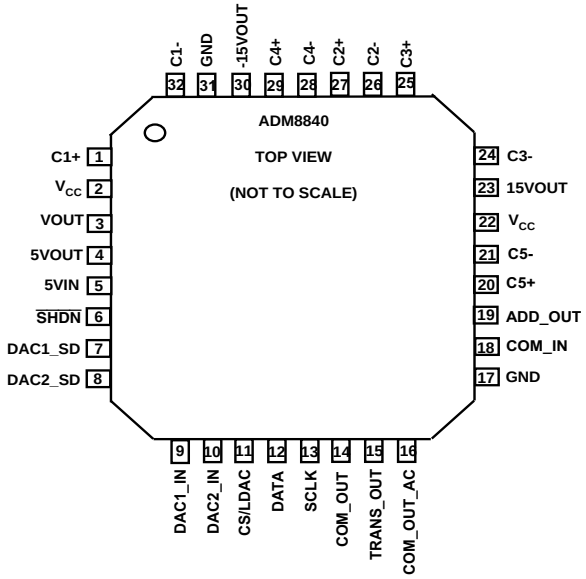
### THERMAL CHARACTERISTICS

32-Lead LFCSP Package:
$\Theta_{JA}$ = 28°C/Watt

### ORDERING GUIDE

| Model | Temperature Range | Package Option |
|---|---|---|
| ADM8840ACP | -40°C to +85°C | CP-32 |

### PIN CONFIGURATION



**PIN FUNCTION DESCRIPTION**

| Pin | Mnemonic | Function |
|---|---|---|
| 1,32 | C1+,C1- | External capacitor C1 is connected between these pins. A 3.3μF capacitor is recommended. |
| 2,22 | $V_{CC}$ | Positive Supply Voltage Input. Connect this pin to 3V supply. A 4.7μF decoupling capacitor should be attached close to pin 2. |
| 3 | VOUT | Voltage Doubler Output. This was derived by doubling the 3V supply. A 3.3μF capacitor to ground is required on this pin. |
| 4 | +5VOUT | +5.0V output pin. This was derived by doubling and regulating the +3V supply. A 2.2μF capcitor to ground is required on this pin to stabilise the regulator. |
| 5 | +5VIN | +5.0V input pin. This is the input to the voltage tripler and inverter charge pump circuits. |
| 6 | $\overline{SHDN}$ | Digital Input. 3V CMOS Logic. Active low shutdown control. This shuts down the timing generator and enables the discharge circuit to dissipate the charge on the voltage outputs, thus driving them to 0V. |
| 7 | DAC1_SD | Switches over to external DAC1 input when asserted. |
| 9 | DAC1_IN | Input for external DAC1 signal. |
| 17, 31 | GND | Device Ground Pin. |
| 13 | SCLK | External Clock Input. Used to load DAC 1 with COM Voltage amplitude and DAC 2 with COM Centre Voltage. |
| 12 | DATA | Digital Data Input to both DAC's 1 and 2. |
| 11 | $\overline{CS}$ / LDAC | Dual function pin.<br>1.Chip Select. Digital Input Logic. Chip Select for Digital Interface.<br>2. Load DAC. Digital Input Logic. DAC's 1 and 2 perform a conversion on a low-to-high transition. |
| 18 | COM_IN | Clock Input from digital controller chip. This input is level shifted, offset and inverted to provide a COM Voltage output swing at a frequency of the COM_IN input. |
| 16 | COM_OUT_AC | COM_OUT_AC outputs the COM_IN signal inverted and level shifted by the value programmed on DAC 1. A 4.7μF capacitor is connected between this pin and COM_OUT. |
| 14 | COM_OUT | The AC output on COM_OUT_AC is added to the center voltage programmed on DAC2 so that the desired amplitude, centered about the correct center voltage appears on COM_OUT. The load capacitance seen by this pin is the bulk capaci tance of the panel, typically 20nF. |
| 8 | DAC2_SD | Switches over to external DAC2 input when asserted. |
| 10 | DAC2_IN | Input for external DAC2 signal. |
| 15 | TRANS_OUT | Level Translator Reference Output Voltage. This is the voltage that the value on DAC 1 is gained up to to provide the upper voltage for the Level Translator. A voltage of between 4.0V and 7.0V can be output here. A 4.7μF cap is recommended for this pin. |

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM8840 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**PIN FUNCTION DESCRIPTION (Contd.)**

| Pin | Mnemonic | Function |
|---|---|---|
| 19 | ADD_OUT | Voltage Adder Output Pin. This is voltage generated by adding VOUT (unregulated output of first stage doubler) to $V_{CC}$. This summed voltage is then used as the supply for the gain stage which generates the Level Translator Output Voltage. A 4.7μF capacitor is recommended for this pin. |
| 20,21 | C5+,C5- | External capacitor C5 is connected between these pins. A 3.3μF capacitor is recommended. |
| 23 | +15VOUT | +15.0V output pin. This was derived by tripling the +5.0V regulated output. A 0.22μF capacitor is required on this pin. |
| 29,28 | C4+,C4- | External capacitor C4 is connected between these pins. A 0.22μF capacitor is recommended. |
| 25,24 | C3+,C3- | External capacitor C3 is connected between these pins. A 0.22μF capacitor is recommended. |
| 27,26 | C2+,C2- | External capacitor C2 is connected between these pins. A 0.22μF capacitor is recommended. |
| 30 | -15VOUT | -15.0V output pin. This was derived by inverting the +15.0V output. A 0.22μF capacitor is required on this pin. |

## COM_OUT VOLTAGE

The COM Driver section of the ADM8840 can be used to generate the alternate frame or line inversion of the COM line of the LCD panel. The ADM8840 receives the COM clock (with frequency up to 10kHz) from the controller and allows programmable conditioning of its amplitude and centre voltage through the use of on-board DAC's 1 and 2. This allows programmable elimination of display flicker caused by the COM inversion.

The COM_OUT amplitude can be programmed from 4.0V to 7.0V in steps of 28mV. The COM_OUT centre voltage can be programmed from 0.9V to 2.8V in steps of 14mV. Figure 1 below shows a typical output from the COM_OUT pin. If programmable operation is not required the DACs can be shutdown with the DAC1_SD and DAC2_SD pins and an analog voltage applied to the DAC1_IN and DAC2_IN pins to set up the amplitude and centre voltage at COM_OUT.

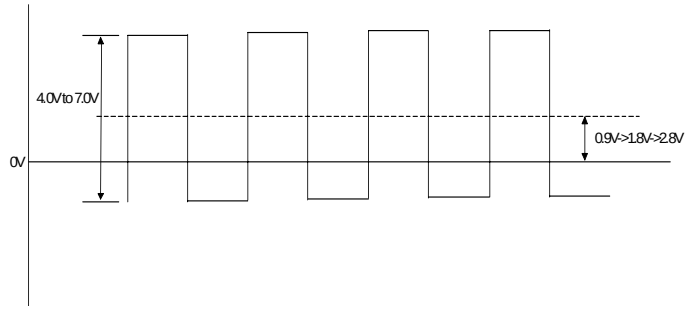



*Figure 1. COM_OUT Voltage*

## POWER SEQUENCING

In order for the TFT panel to power up correctly, the gate drive supplies must be sequenced such that the -15V supply starts up before the +15V supply. The ADM8840 controls this sequence. When the device is turned on, the ADM8840 allow the -15V output to ramp immediately, but holds off the +15V output. It continues to do this until the negative output has reached -3V. At this point, the positive output is enabled and allowed to ramp to +15V. This sequence is highlighted in figure 2.

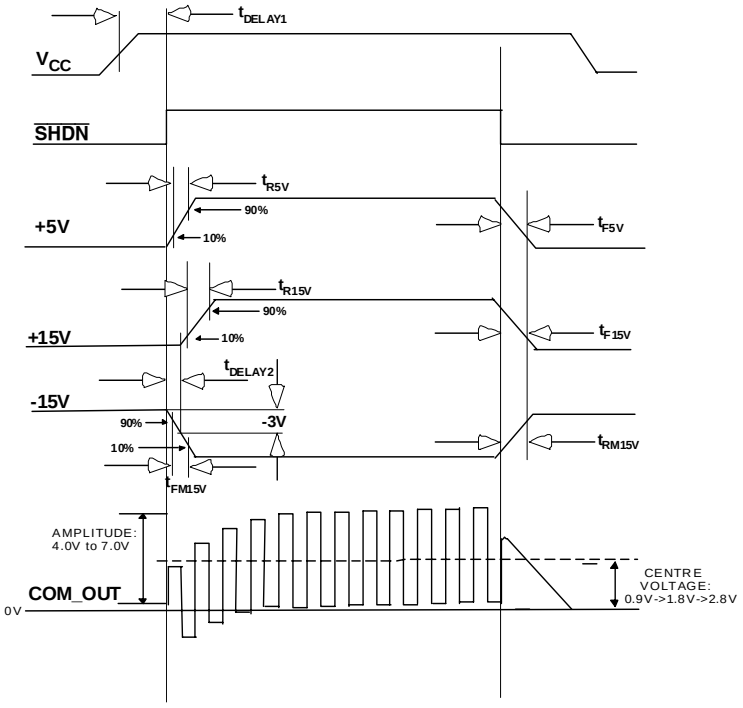



*Figure 2. Power Sequence*

**SERIAL INTERFACE**

The COM Driver section of the ADM8840 uses a serial interface to input data and transfer it into the DACs. Figure 3, below, shows the operation of the serial interface. The data is transmitted along the serial DATA line, along with a serial clock signal, SCLK. This data is read into a Shift Register. When the 8 bits are sucessfully stored in the Shift Register a low-to-high transition on the CS/LDAC input causes the latch to load the 8-bits of data into the relevent DAC.

This function is also shown in the waveforms in Figure 4 below. A falling edge on the CS/LDAC input initiates the data read into the shift register. The first bit of the datastream is the DAC Select Bit (DAC_SEL) which determines which internal DAC the data will be written to. A '1' selects DAC 1 which sets the Amplitude of the output and a '0' selects DAC 2 which sets the Centre Voltage of the output. The individual data bits are then read in one by one on the DATA line. After the DAC_SEL bit and the 8 data bits have been read there is a pause to ensure the shift register outputs are stable. Then a rising edge on the CS/LDAC input loads the 8 bits on the shift register outputs into the relevent DAC (and the DAC outputs will change accordingly). Note that if CS/LDAC goes high before all 8 data bits are read in then incorrect data will be loaded into the DACs. All bits on the DATA line are read in on each rising edge of the SCLK signal.

When the ADM8840 comes out of shutdown the DACs are preset with default values generating a COM_OUT Amplitude of 6V with a Centre voltage of 1.5V.

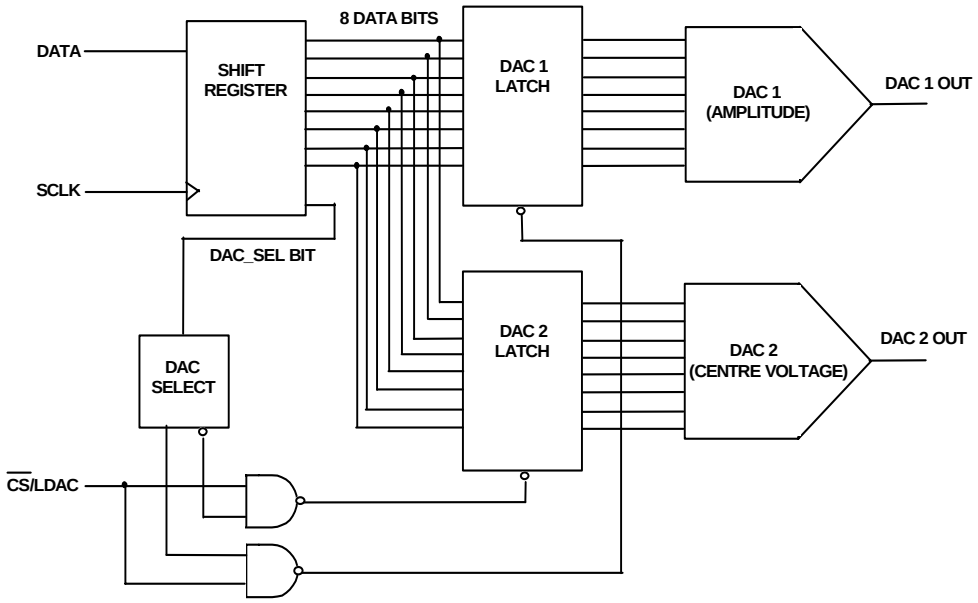



*Figure 3. Serial Interface Diagram*

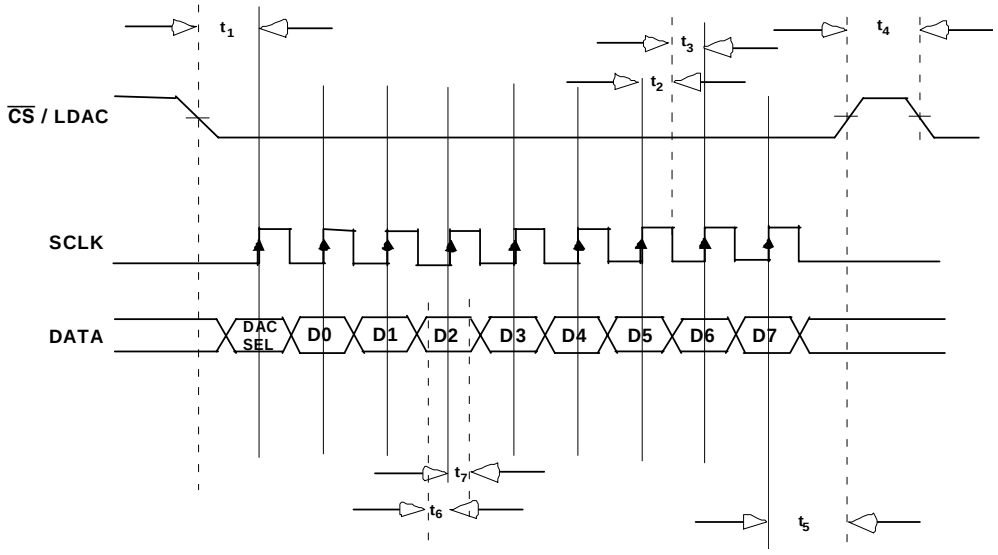



*Figure 4. Serial Interface Waveforms*

**DAC1 Setup**

The resolution of DAC1 is 4.7mV this is scaled up by 6 to give COM_OUT amplitude resolution of 28mV (4.7mV * 6 = 28mV). The COM_OUT amplitude Vp-p is given by, (Binary Code/255)(1.188)(6)= Vp-p (COM_OUT).

A table of the min, max and typical values for COM_OUT amplitude is given in the Table 1 below.

**DAC2 Setup**

The resolution of DAC2 is 4.7mV this is scaled up by 3 to give you the COM_OUT centre voltage resolution of 14mV (4.7mV * 3 = 14mV). The COM_OUT centre voltage is given by,

(Binary Code/255)(1.188)(3)= COM_OUT DC Voltage.

A table of the min, max and typical values for COM_OUT centre voltage is given in the Table 2 below.

Table 1 COM_OUT amplitude Voltage

| COM_OUT amplitude voltage | | Binary Bits written to DAC1 | Integer | DAC1_IN Voltage |
|---|---|---|---|---|
| (Max) | 7.016V | 11111011 | 251 | 1.667V |
| | 6.9882 | 11111010 | 250 | 1.6623 |
| | ..... | ..... | ..... | ..... |
| (Typ) | 6.0098V | 11010111 | 215 | 1.0011V |
| | ..... | ..... | ..... | ..... |
| | 4.0531V | 10010001 | 145 | 671.7mV |
| (Min) | 4.0025V | 10010000 | 144 | 667mV |

Table 2 COM_OUT centre voltage

| COM_OUT centre voltage | | Binary Bits written to DAC2 | Integer | DAC2_IN Voltage |
|---|---|---|---|---|
| (Max) | 2.8092V | 11001001 | 201 | 933mV |
| | 2.7952V | 11001000 | 200 | 928mV |
| | ..... | ..... | ..... | ..... |
| (Typ) | 1.5094V | 01101100 | 108 | 503.9mV |
| | ..... | ..... | ..... | ..... |
| | 0.9224V | 01000010 | 66 | 304.7mV |
| (Min) | 0.9084V | 01000001 | 65 | 300mV |

## BOOSTING THE CURRENT DRIVE OF THE +/-15V SUPPLY

The ADM8840 +/-15V output can deliver 100uA of current in the typical configuration, as shown in Figure 5.

In this configuration the 5Vout (pin 4) is connected to 5Vin (pin 5), as can be seen on block diagram Page 1 of this data sheet.

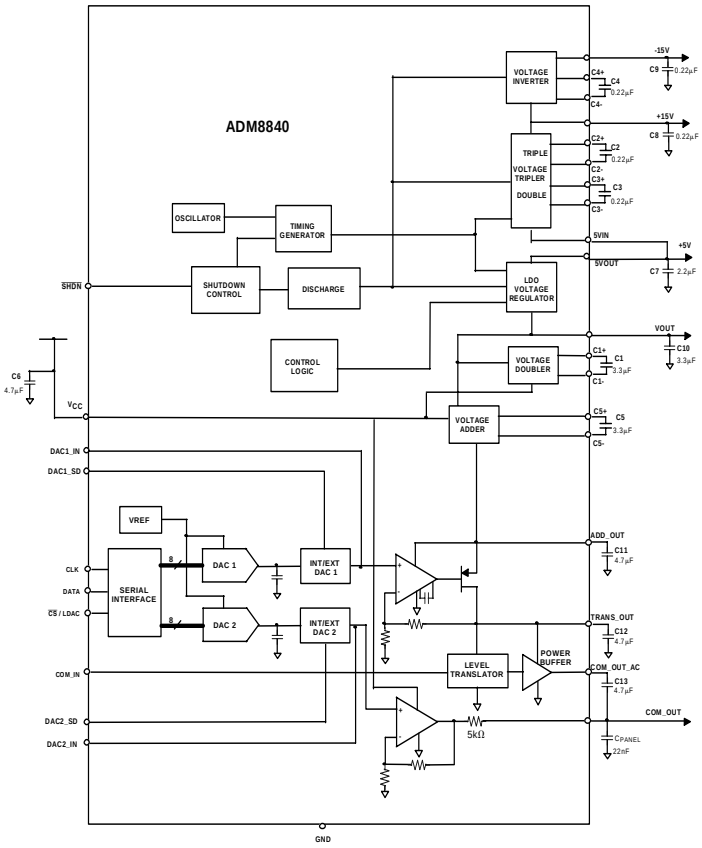



Figure 5. Typical Configuration

It is possible to configure the ADM8840 to supply up to 400uA on the +/-15V outputs, by changing its configuration slightly, as shown in Figure 6.

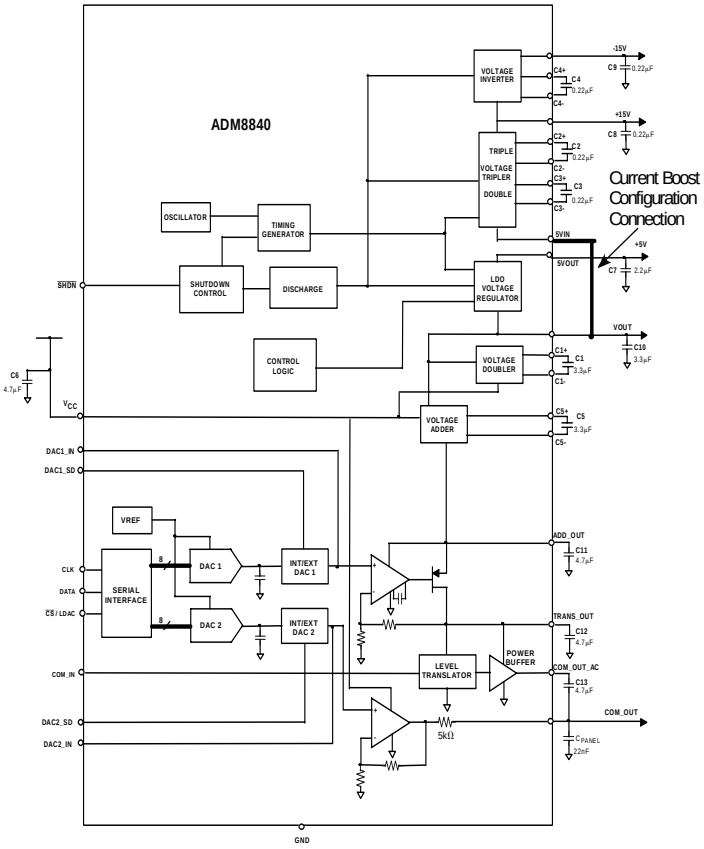



Figure 6. Current Boost Configuration

The configuration in Figure 6, can supply up to 400uA of current on both the +15V and the -15V outputs. If the load on the +/-15V does not draw any current the voltage on the +/-15V outputs can rise up to +/-16.5V.In this configuration Vout (pin 3) is connected to 5Vin (pin 5).

# ADM8840

## OUTLINE DIMENSIONS

Dimensions Shown in Inches and (mm).

### 32-Lead 5X5 Chip Scale Package (CP-32)